HEWLETT PACKARD

Memory Expansion Module Diagnostic

reference manual

For HP 1000 M/E/F-Series
Dynamic Mapping Systems

ABSOLUTE BINARY PROGRAM NO. 12929-16001
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PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, Update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past Updates, however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all Updates.

To determine what software manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

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SECTION I

INTRODUCTION

1-1. GENERAL

This diagnostic confirms proper operation of the HP 12976A and 13305A/13307A Dynamic Mapping Systems for HP 1000 Computers. This diagnostic is used in conjunction with the diagnostic configurator, and communicates with the operator via the hardware registers and the system console.

The test method consists of executing the instructions under test, and comparing the results to predetermined or calculated values or tables in memory. This involves the use of many CPU base set instructions as well as some extended instruction group instructions. Therefore, this diagnostic should be run only after the following diagnostics have been successfully executed:

a. Memory Reference Instruction Diagnostic
b. Alter-Skip Instruction Diagnostic
c. Shift-Rotate Instruction Diagnostic
d. Extended Instruction Group Diagnostic
e. I/O Instructions and Interrupt Diagnostic
f. Semiconductor Memory Diagnostic
g. Direct Memory Access Diagnostic
h. Memory Protect/Parity Error Diagnostic

} Part of Diagnostics on Multimedia HP 24396A-F

1-2. REQUIRED HARDWARE

The following hardware is required:

An HP 1000 Computer with at least 16K bytes of memory and with register display capability.

An HP 12976A/B (M-Series) or HP 12731A (E/F-Series) Dynamic Mapping System.

An HP 12566B/C Microcircuit Interface PCA. (See paragraph 3-1 for jumper settings.)

An HP 1251-0332 24 pin printed circuit connector with pins 22 and 23 wired together.

A diagnostic input device (for loading program only).

A console device for message reporting is optional.

1-3. REQUIRED SOFTWARE

The following software is required:

DIAGNOSTIC	MANUAL PART NUMBER	ABSOLUTE BINARY PROGRAM NUMBER
Diagnostic Configurator	02100-90157	24296-60001
Memory Expansion Module Diagnostic	12929-90003	12929-16001

The diagnostic serial number of this diagnostic, which resides in memory location 126 (octal), is 102003.

SECTION II

PROGRAM ORGANIZATION

2-1. ORGANIZATION

The diagnostic program consists of 22 tests plus the control and initialization sections, which accept the select code and options required by the tests. The tests are called into execution by the control section as sequential or selectable subroutines. The following instructions and circuits are placed under test by this diagnostic:

1.	Maps — XMM Transfer Maps or Memory	TST00
2.	Maps — XMS Transfer Maps Sequentially	TST01
3.	Maps — XMA/B Transfer Maps Internally	TST02
4.	Maps — SYA/B, USA/B, PAA/B, PBA/B (Load/Store Maps)	TST03
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20.	Extended Memory Test (Utility)	TST23
21.	Basic I/O (Utility	TST24
22.	Register Crusher Test	TST25

2-2. TEST CONTROL AND EXECUTION

The program outputs a title message with the DSN to the console device for operator information and then executes the tests according to the options selected on the Switch Register by the operator. The program also keeps count of the number of passes that have been completed and will output the pass count at the completion of each pass. The pass counter will be reset if the program is restarted.

2-3. SELECTION OF TESTS BY OPERATOR

The operator has the capability to select one particular test or a sequence of tests. Paragraph 3-5 outlines the operator test selection capability.

2-4. MESSAGE REPORTING

There are two types of messages output for diagnostics: error and information. Error messages are used to inform the operator when the device fails to respond to a given instruction or control sequence. Information messages are used to inform the operator of the progress of the diagnostic or to instruct the operator to perform some task(s) related to the operation of the unit. In the latter case, an associated halt will occur to allow the operator time to perform the task. The operator must then press RUN. If a console device is used, the printed message will be preceded by the letter E (error) or the letter H (information) and a number (in octal). The number is also related to the halt code when a console device is not available. Examples of error and information messages are as follows (specific meanings are listed in section IV):

Example — Error with halt

Message: E013 SECOND INT OCCURRED
Halt Code: 102013 (octal) (T-Register)

Example — Information with halt

Message: H024 PRESS PRESET (EXT & INT), RUN
Halt Code: 102024 (octal)

Example — Information only

Message: H025 BI-O COMP
Halt Code: None

Error messages can be suppressed by setting Switch Register bit 11 and error halts can be suppressed by setting Switch Register bit 14. This is useful when looping on a single section that has several errors. Information messages are suppressed by setting Switch Register bit 10.

Operator intervention is suppressed by setting Switch Register bit 8 (i.e., Preset Test in BI-O). When Switch Register bit 12 is set the tests that are selected will be repeated, and all operator intervention will be suppressed.

2-5. DIAGNOSTIC LIMITATIONS

If an error is detected, the diagnostic cannot tell whether the hardware or firmware was the cause of the error, because this diagnostic requires the microprocessor to execute its Dynamic Mapping System instruction set. If the operator suspects that the microprocessor is at fault, a thorough test of the microprocessor is in order before continuing with this diagnostic.

Since it is possible to be mapped into nonexistant or incorrect memory locations if a hardware fault is present, the operator may find that the diagnostic halt displayed is part of a test which was not selected. It is also possible that the computer will stay in the RUN mode, but not executing the diagnostic, due to problems with incorrect mapped jumps etc; therefore, the operator should remember that running time of the standard set of tests in the diagnostic is less than 16 seconds. This includes the 10 seconds required for the Preset test.

SECTION III

OPERATING PROCEDURE

3-1. MICROCIRCUIT INTERFACE JUMPER CONFIGURATION

The following gives the jumper configurations allowed for the HP 12566B/C Microcircuit Interface PCA (Ground True or +True I/O) required as a data transfer/interrupt device:

	12566B	12566C
W1	C	C
W2	B	B
W3	B	B
W4	B	B
W5	IN	OUT
W6	IN	OUT
W7	IN	OUT
W8	IN	OUT
W9	A	A
W10	NA	B
W11	NA	IN
W12	NA	OUT
W13	NA	OUT

3-2. OPERATING PROCEDURES

A flowchart of the operating procedures for loading the Diagnostic Configurator and this diagnostic is provided in figure 3-1.

If an unconfigured Diagnostic Configurator is available, start at entry point A on the flowchart.

If a configured Diagnostic Configurator is available, start at entry point B on the flowchart.

If a combined configured Diagnostic Configurator and an unconfigured Diagnostic is available, start at entry point C on the flowchart.

If a combined configured Diagnostic Configurator and a configured Diagnostic is available, start at entry point D on the flowchart.

3-3. RUNNING THE DIAGNOSTIC

The program will now execute the diagnostic according to the options selected in the Switch Register. (See table 3-1.) If the Switch Register is cleared, all standard tests will be executed. At the completion of each pass of the diagnostic, the pass count is printed on the console device to inform the operator. The computer halts with 102077 displayed in the T-register and the pass count is contained in the A-register. At this point, the operator need only press RUN to execute another pass of the diagnostic.

If Switch Register bit 12 was set, the number of passes is printed and the diagnostic control program will restart the execution of the selected test(s).

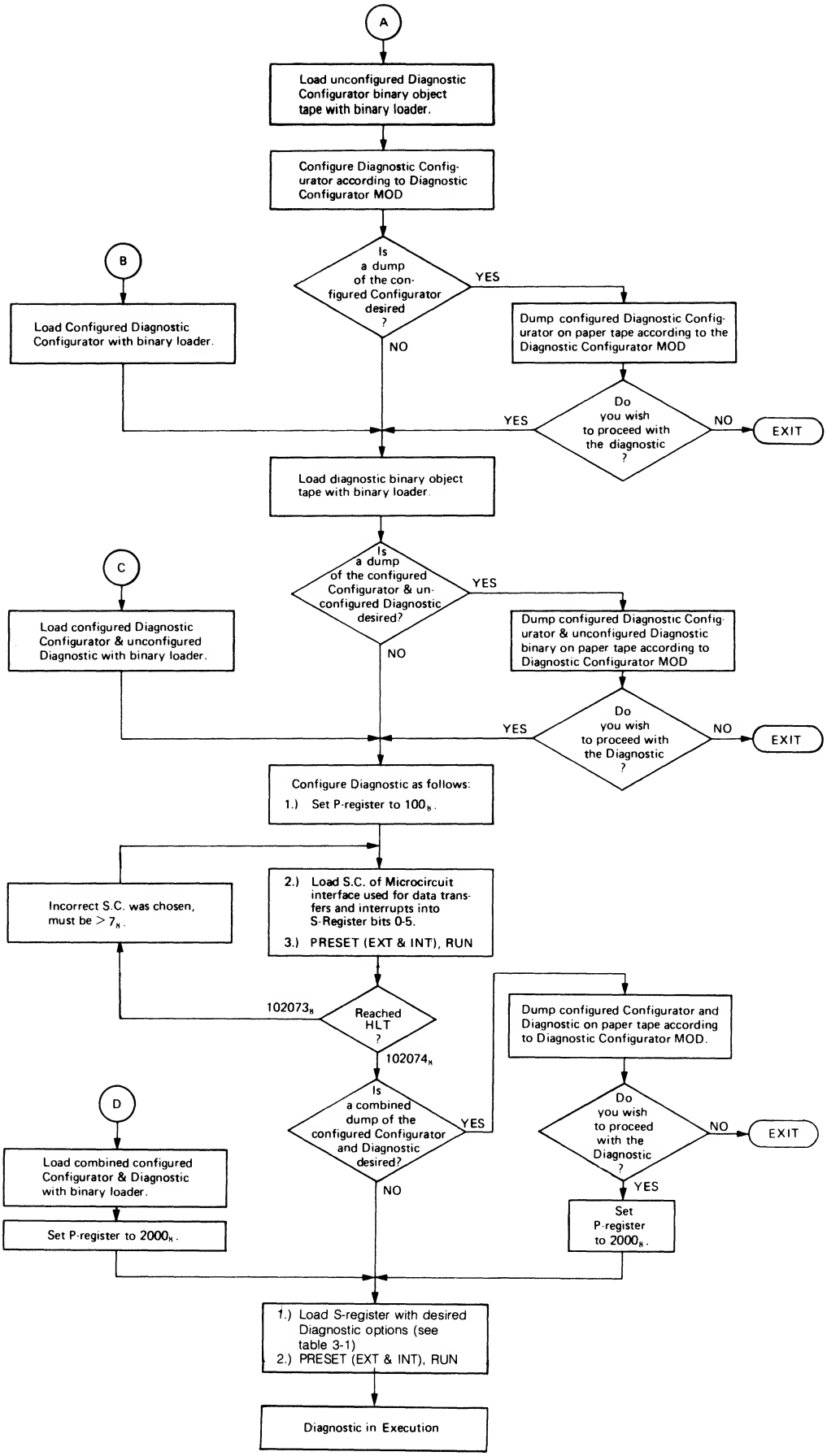

Figure 3-1. Operating Procedure Flowchart

Table 3-1. Switch Register Options

BIT	MEANING IF SET
15	Halt (102076) at the end of each test; the A-Register will contain the octal equivalent of the test just completed.
14	Suppress error halts.
13	Repeat last test executed (loop on test).
12	Repeat all selected tests after diagnostic run is complete without halting. The end of pass message "PASS XXXXX" will be output before looping. Also suppresses tests requiring operator intervention.
11	Suppress error messages.
10	Suppress information messages.
9	Abort the current diagnostic execution and halt (102075); user may at this time specify a new set of tests in the A/B-register, clear bit 9 of the Switch Register, and press RUN.
8	Suppress tests requiring operator intervention.
7-0	Reserved.

3-4. RESTARTING THE DIAGNOSTIC

The program may be restarted by setting the P-register to 2000 (octal), selecting the desired Switch Register options, and pressing RUN.

If a trap cell halt (106077 octal) occurs, the user must determine the cause of the interrupt or transfer of control to the location shown in the M-register. The program may need to be reloaded to continue.

3-5. TEST SELECTION

The Control portion of the program provides the operator with a method to select a single test or sequence of tests to be run. The operator sets Switch Register bit 9 to indicate that a selection is desired. If the computer is halted, press RUN. The computer will come to a halt 102075 (octal) to indicate ready for selection. If the diagnostic is running, the test in progress will be completed; then the program will halt.

After the halt, the operator may select the desired test(s) by setting the A- and B-register value equal to the desired test numbers. A-register bit 0 represents Test 00, bit 1 represents Test 01, etc. For a definition of tests, see table 3-2.

After pressing "RUN" the selected test(s) will be run. To run the standard test (see table 3-2 for standard test set) after special selection, the operator need only set the A- and B-register to zero.

Table 3-2. Test Selection Summary

A-REGISTER BIT	IF SET WILL EXECUTE
0	TEST 00
1	TEST 01
2	TEST 02
3	TEST 03
4	TEST 04
5	TEST 05
6	TEST 06
7	TEST 07
8	TEST 10
9	TEST 11
10	TEST 12
11	TEST 13
12	TEST 14
13	TEST 15
14	TEST 16
15	TEST 17
B-REGISTER BIT	**IF SET WILL EXECUTE**
0	TEST 20
1	TEST 21
2	TEST 22
3*	TEST 23
4*	TEST 24
5*	TEST 25
6-15	RESERVED

*Tests 23, 24 and 25 are not part of the standard run; these tests must be selected by the operator.

SECTION IV

DIAGNOSTIC PERFORMANCE

4-1. TEST DESCRIPTION

Tests 00 through 25 (octal) are described in following paragraphs. Refer to table 4-2 (comments on halt codes) for additional details on the content of each test.

4-2. XMM TEST (TST00)

This test verifies proper operation of the hardware and firmware required to execute an XMM instruction. Test 00 is made up of four subtests: Register Address, single map pattern, boundary area, and entire map area.

Subtest 1 — Register Address Test

The register address test diagnoses one register at a time. Starting with register 0, the register is loaded with 0, then read back and verified. Then register 1 is loaded with a 1, and so on. When the final register (177 octal) is loaded and read back, the subtest passes control to subtest 2.

Subtest 2 — Single Map Pattern Tests

When all registers have been individually loaded, read, and verified for load/read ability, each map is tested, using various patterns, such as all zeros, all ones, and alternating ones-zeros, before this subtest passes control to subtest 3.

Subtest 3 — Boundary Area Tests

After it is verified that all four maps have load/read ability, the ability of XMM to cross map boundaries is tested. The six registers on each side of the map boundaries are loaded and read back using a single instruction. When all three boundary areas have been tested, control is passed to subtest 4.

Subtest 4 — Entire Map Area Test

All four maps are tested next as a single address space using a word count of 177 (octal) with XMM and the test exits to the control program.

If an error is detected during the execution of Test 00, an error message is output on the console, and the program halts the computer. At this time the operator may determine the cause of the error by checking the following registers:

T-Register = Error Code
A-Register = Actual Pattern
B-Register = Expected Pattern
X-Register = Failing Register Number
Y-Register = Failure Address

4-3. XMS TEST (TST01)

This test verifies proper operation of the hardware and firmware required to execute an XMS instruction. Each map is individually addressed and loaded then read back using XMS. The success of the operation is verified by a routine called TBCMP (Table Compare), which compares the two memory tables used in the load/read operation. When each map has been successfully verified, all four maps are addressed in one operation, loaded, read, and verified. Then the test passes control back to the control program.

If an error is detected during the execution of Test 01, an error message will be output on the console, and the program will halt the computer. At this time, the operator can determine the cause of the error by checking the following registers.

T-Register = Error Code
A-Register = Actual Pattern
B-Register = Expected Pattern
X-Register = Failing Register Number
Y-Register = Error Address

4-4. XMA/B TEST (TST02)

This test exercises the hardware and firmware required for the execution of the XMA and XMB instructions. This test consists essentially of eight subtests, each of which verifies one function of the XMA/XMB instructions. These tests are:

1. Transfer the contents of the System map to the Port A map using XMA.
2. Transfer the contents of the System map to the Port B map using XMA.
3. Transfer the contents of the User map to the Port A map using XMA.
4. Transfer the contents of the User map to the Port B map using XMA.
5. Transfer the contents of the System map to the Port A map using XMB.
6. Transfer the contents of the System map to the Port B map using XMB.
7. Transfer the contents of the User map to the Port A map using XMB.
8. Transfer the contents of the User map to the Port B map using XMB.

Upon the completion of each transfer, the Port A or Port B map is read into memory and tested for a proper transfer. When these eight tests have been completed, Test 02 passes control back to the control program.

If an error is detected during execution of Test 02, an error message will be output on the console, and the program will halt the computer. At this time, the operator can determine the cause of the error by checking the contents of the following registers:

T-Register = Error Code
A-Register = Actual Pattern
B-Register = Expected Pattern
X-Register = Failing Register Number
Y-Register = Failure Address

4-5. LOAD/READ MAPS INSTRUCTIONS TEST (TST03)

This test verifies the ability of MEM to successfully execute the following instructions:

1. SYA — load/read System map from/to an A-register pointer
2. SYB — load/read System map from/to a B-register pointer
3. USA — load/read User map from/to an A-register pointer
4. USB — load/read User map from/to a B-register pointer
5. PAA — load/read Port A map from/to an A-register pointer
6. PAB — load/read Port A map from/to a B-register pointer
7. PBA — load/read Port B map from/to an A-register pointer
8. PBB — load/read Port B map from/to a B-register pointer

Each of these instructions are used to load and then read its associated map area, and the results are tested to verify proper execution. The pattern loaded by the A-register reference instruction is changed prior to the execution of the B-register reference counterparts.

When all eight instructions have been tested, a test is made to ensure that the execution of one of these instructions does not alter the contents of the other three map areas. After completion of this interference check, Test 03 passes control back to the control program.

If an error is detected while executing Test 03, the error code and failing instruction are output on the console, and the program halts the computer. At this time, the operator can determine the cause of the error by examining the following registers:

T-Register = Error code
A-Register = Actual Pattern
B-Register = Expected Pattern
X-Register = Failing Register Number
Y-Register = Failure Address

4-6. STATUS-FENCE TEST (TST04)

This test verifies proper operation of the hardware and firmware of the MEM status register and the following instructions:

1. DJP — Disable MEM and Jump
2. DJS — Disable MEM and Jump Subroutine
3. SJP — Enable System map and Jump
4. SJS — Enable System map and Jump Subroutine
5. UJP — Enable User map and Jump
6. UJS — Enable User map and Jump Subroutine
7. RSA/B — Read Status into A/B-register
8. LFA/B — Load Fence from A/B-register
9. SSM — Store Status in Memory
10. JRS — Jump and Restore Status

Test 04 checks the status register bits by executing one of the above instructions, the interrupt system, and the protect features of MEM to establish validity of the various status register bits.

The initial checking is done through the A-register referencing RSA and LFA instructions. Once it is established that the A-register referenced instructions work properly, the B-register counterparts are checked. After all bits of the status register are checked, control is returned to the control program.

If an error is detected during the execution of Test 04, an error message will be output on the console, and the program will halt the computer. At this time, the operator may determine the cause of the error by examining the following registers:

T-Register = Error Code
* A-Register = Status Bit(s) which failed
* B-Register = Status Bit(s) which failed
X-Register = Contents of Status Register at Failure
Y-Register = Failure Address

* The actual status bit will be found in the register referenced by the instruction, and expected state of the bit will be found in the alternate register.

4-7. CROSS STORE-LOAD-COMPARE TEST (TST05)

This test verifies the ability of the hardware and firmware to perform the execution of the following instructions:

1. XSA/B — Cross Store from A/B to Alternate map
2. XLA/B — Cross Load to A/B from Alternate map
3. XCA/B — Cross Compare A/B with Alternate map

These instructions function in the same manner as the base set store-load-compare instructions.

Subtest 1 — A-Register Reference Instructions

This subtest enables the System map and cross stores a pattern to a User map address. Next, the MEM is disabled and the contents of the cross stored address are directly loaded using LDA instruction from the physical address (different from the logical address) and then compared for a successful cross store operation. Next, the System map is re-enabled and a cross load is executed and compared with the data pattern which was stored. Upon verifying the pattern cross loaded into the A-register, a cross compare is executed, thus verifying the three instructions (XSA, XLA, and XCA) work correctly for the pattern at that address.

The pattern is then changed, and the same sequence is executed. After it is determined that the above instructions work correctly for both patterns crossing from the system to the User map, the User map is enabled and the same sequences are used to test XSA, XLA, and XCA, from the User to the System map. Control is then passed to subtest 2.

Subtest 2 — B-register Reference Instructions

XSB, XLB, and XCB are verified in the same sequence of tests as described in Subtest 1 and control passes to subtest 3.

Subtest 3 — Multiple Cross Stores-Loads-Compares

A counter is set up, and 50 cross stores are executed (25 each XSA and XSB instructions) with the System map enabled. The counter is set to zero, and 50 cross loads (25 each XLA and XLB instructions) are executed with a compare routine after each cross load. Next, 50 cross compares (25 each XCA and XCB instructions) are executed. The User map is then enabled and the above sequence of instructions is repeated. Control is then passed back to the control program.

If an error is detected during execution of Test 05, the error message will be output on the console, and the program will halt the computer. At this time, the operator may determine the cause of the error by examining the following registers:

T-Register = Error Code
* A-Register = Pattern
* B-Register = Pattern
X-Register = Physical Target Address of Instruction
Y-Register = Address of Failing Instruction

* The actual pattern will be found in the register referenced by the cross instruction, and the expected pattern will be found in the alternate register.

4-8. MOVE WORDS TEST (TST06)

This test verifies proper operation of the hardware and firmware required to execute the following instructions:

1. MWF — Move Words From alternate map
2. MWI — Move Words Into alternate map
3. MWW — Move Words Within alternate map

These macroinstructions move a string of words using the alternate map as the source and/or destination. The execution of a MWF macroinstruction moves a string of words using the alternate map as a source and the currently enabled map as the destination. The execution of a MWI macroinstruction moves a string of words using the currently enabled map as a source and the alternate map as the destination. The execution of an MWW macroinstruction moves a string of words with both the source and destination addresses established through the alternate map.

Test 06 is made up of three subtests: (1) a set of tests to exercise the MWF macroinstruction; (2) a set of tests to exercise the MWI macroinstruction; and (3) a set of tests to exercise the MWW macroinstruction.

Subtest 1 — Move Words From

This subtest begins by writing a "memory address" test in the source addresses, and zeroing the destination addresses. A test is run moving the first 10 words from the alternate map and verifying their contents, then the entire page is moved and verified. Next, the ability to move words crossing page boundaries is tested.

Finally, a pointer and counter are established, 10 patterns are moved (one page at a time) and verified, and control is passed to the next subtest.

Subtest 2 — Move Words Into

This subtest begins with the "memory address" routine written into the source area and the following tests are made:

1. Move 10 words to User area
2. Move 1024 words to User area
3. Move 100 words (50 on each side of a page boundary) to User area
4. Move 10 patterns of 1024 words each to User area
5. Move 10 words to System area
6. Move 1024 words to System area
7. Move 100 words to System area (across the page boundary)
8. Move 10 patterns of 1024 words each to System area

The system and user map areas are enabled and disabled as required by the program to use the MWI instruction and the various routines to compare and report errors if detected.

Subtest 3 — Move Words Within

This subtest moves one word within the User map from the system, then one word is moved within the System area from the User area. Next, 100 words are moved within the User area. They are verified for proper completion with the MWW instruction 100 words are moved within the system and checked and finally, one page (1024) words are moved and verified, a different pattern written into the source and the routine is repeated 10 times.

When the three subtests have been successfully completed, the control is passed back to the executive program.

If an error is detected during the execution of Test 06, an error message is output on the console, and the program will halt the computer. At this time the operator may determine the cause of the error by examining the following registers:

T-Register = Error Code
A-Register = Actual Pattern
B-Register = Expected Pattern
X-Register = Physical Address of Failure
Y-Register = Failure Address

4-9. MOVE BYTES TEST (TST07)

Test 07 verifies proper operation of the hardware and firmware required to execute the following instructions:

1. MBF — Move Bytes From alternate map
2. MBI — Move Bytes Into alternate map
3. MBW — Move Bytes Within alternate map

These macroinstructions move a string of bytes using the alternate program map as the source and/or destination.

Test 07 is comprised of three subtests, and follows the test path used in Test GG (Move Words Test). Error detection and reporting are the same as explained in the Test 06 description.

4-10. PROTECTED MODE PRESET TEST (TST10)

Test 10 verifies proper operation of the hardware and firmware required to set and clear MEM status register bit 11 (protected mode), and the base page fence. This test starts by setting the protected mode, checking the MEM status register for the correct state of bit 11. The protected mode is then forced off programatically and the state of status register bit 11 is again tested.

If the protected mode cannot be turned off either programmatically or by pressing HALT-PRESET, then neither a halt nor an error message is possible. To inform the operator of this condition, the Extend Register is flashed on and off at approximately one-half second intervals. If this condition exists, the operator must press halt again, and correct the problem before continuing the diagnostic.

The message "H115 PRESS HALT,PRESET,RUN IN LESS THAN 10 SECONDS" is output on the console, the protected mode is again set, and the program starts a 10-second timer.

The operator must then press HALT, PRESET, and RUN. The state of status register bit 11 is tested to verify that preset turns the protected mode off, and the base page fence is tested to ensure that preset also zeros the base page fence. Then the test exits to the control program.

If an error is detected during the execution of TST10, the message "E114 PM NOT SET BY STC 05" or "E116 PM OR MEM FENCE NOT CLEARED BY PRESET" will be output on the console, and the program will either halt the computer or the flashing E-register will occur.

If no console was configured during Diagnostic Configurator initialization, the program causes the computer to halt with 107026 displayed in the T-register. This will inform the operator that the Protected Mode Preset Test is next, and he must press RUN to start the test.

4-11. VIOLATIONS TEST (READ/WRITE/BASE PAGE) (TST11)

Test 11 verifies proper operation of the hardware and firmware required to identify and report unprotected mode violations caused by trying to load, store, or enter areas of memory which are designated as protected by the DMS. This test includes the following three subtests.

Subtest 1 — Read Violation Test (Violation Register Bit 15)

Protected Mode (PM) is set and a read is attempted. Then the program ensures that a MEM violation (MEMV) occurred, and that the read was not allowed.

Subtest 2 — Write Violation Test (Violation Register Bit 14)

PM is set and a write into a protected area of memory is attempted. The tests are once again made to ensure a MEMV occurred, and that the write was disallowed.

Subtest 3 — Base Page Fence Violation Test (Violation Register Bit 13)

PM is set and the program tries to write and then jump under the base page fence. In both cases, MEMV is tested and the program ensures that the attempts were denied access within the boundaries of the MEM base page fence.

If an error is detected during the execution of Test 11, the program will output an error message on the console. At this time, the operator may determine the cause of the error by checking the T-register, which will contain the error code, and the Y-register, which will contain the address of the failure.

4-12. WRITE VIOLATIONS TEST (TST12)

Test 12 verifies proper operation of the hardware and firmware required to successfully detect and report a protected mode write violation, as well as prevent the write operation from altering protected memory.

This test includes five subtests, each of which first attempts a write into protected memory, ensures that the protect features cause a MEMV, and then checks to ensure that the write did not change memory. The five instructions used for Test 12 are: MBI, MBW, MWI, MWW, and XSA.

If an error is detected during the execution of Test 12, an error message will be output on the console and the program will halt the computer. The operator may then determine the cause of the error by checking the T-register, which will contain the error code, and the Y-register, which will contain the address of the failure.

4-13. PRIVILEGED INSTRUCTION VIOLATION TEST (TST13)

Test 13 verifies proper operation of the hardware and firmware required to successfully detect and report a protected mode privileged instruction violation.

This test is made up of eight subtests, each of which ensures privileged instructions will cause MEMV interrupts if the User map is enabled, and will not cause violations if the System map is enabled. The instructions used for this test are: JRS, DJP, DJS, SJP, SJS, UJP, UJS, and LFA.

If an error is detected during the execution of this test, an error message will be output on the console and the program will halt the computer. The operator may then determine the cause of the error by checking the T-register, which will contain the error code, and the Y-register, which will contain the address of the error.

4-14. MAPS VIOLATIONS TEST (TST14)

Test 14 verifies proper operation of the hardware and firmware required to detect the attempt, report the attempt, and prevent the execution of any MEM instruction which attempts to alter the contents of the maps while in the protected mode.

This test includes seven subtests, each of which first attempts to alter the contents of the maps, and then ensures that the protect features of the MEM cause an MEMV interrupt and test the violation register to ensure that privileged instruction bit 12 is set. The seven instructions used to attempt alteration of the maps in this test are: XMM, XMS, XMA, SYA, USA, PAA, and PBA.

If an error is detected during the execution of this test, an error message is output on the console and the program halts the computer. At this time, the operator may determine the cause of the error by checking the T-Register, which will contain the error code, and the Y-Register, which will contain the address of the error.

4-15. DCPC PORTS ENABLE TEST (TST15)

Test 15 verifies proper operation of the hardware and firmware required to enable the Port A and Port B maps during a mapped DCPC transfer.

This test includes two subtests which cause DCPC transfers, and check the appropriate mapped addresses to ensure the correct port map was enabled by the DCPC.

If an error is detected during execution of Test 15, an error message will be output on the console and the program will halt the computer. At this time, the operator can determine the cause of the error by checking the following registers:

Y-Register = Failure Address
A-Register = Actual Pattern
B-Register = Expected Pattern
X-Register = Physical Address of Expected Pattern

4-16. READ VIOLATIONS TEST (TST16)

Test 16 verifies proper operation of the hardware and firmware required to successfully detect and report a protected mode read violation.

This test includes four subtests, each of which first attempts a read from protected memory, and then ensures that the protect features of the MEM cause an MEMV interrupt and test the violation register to ensure that read violation bit 15 is set. The four instructions used for Test 16 are: MWW, MWI, MBW, and MBI.

If an error is detected during the execution of this test, an error message will be output on the console and the program will halt the computer. The operator may then determine the cause of the error by checking the T-register, which will contain the error code, and the Y-register, which will contain the address of the failure.

4-17. INTERRUPTIBLE INSTRUCTIONS TEST (TST17)

Test 17 verifies proper operation of the hardware and firmware required to complete the execution of an instruction which has been interrupted by the CPU.

This test includes eight subtests, each of which starts the execution of an interruptible instruction, and then causes an interrupt. At the completion of the interrupt handling routine, control is returned to the interrupted instruction and the results of the instruction under test are checked to verify proper completion. The instructions tested are: MBF, MBI, MBW, MWF, MWI, MWW, XMS, and XMM.

If an error is detected during the execution of this test, an error message is output on the console and the program halts the computer. At this time, the operator can determine the cause of the error by checking the T-register, which will contain the error code, and the Y-register, which will contain the address of the error.

4-18. DCPC INTERFERENCE TEST (TST20)

Test 20 verifies proper operation of the hardware and firmware required to successfully load and read map registers while executing DCPC transfers.

This test executes USA and USB instructions while the DCPC is transferring data and checks the results. If no error is found for every combination of map register load, the test is exited. If an error is detected during the execution of this test, a message is output on the console and the program halts the computer. At this time, the operator may determine the cause of the error by checking the following registers:

T-Register = Halt Code
A-Register = Actual Pattern
B-Register = Expected Pattern
X-Register = Failing Register
Y-Register = Failure Address

4-19. VIOLATION REGISTER MAP BITS TEST (TST21)

Test 21 verifies proper operation of the hardware and firmware required to identify the page on which a violation has occurred.

This test causes several violations to be reported, and tests the violation register map bits for correct value.

If an error is detected during the execution of this test, an error message is output on the console and the program halts the computer. At this time, the operator may determine the cause of the error by checking the contents of the following registers:

T-Register = Error Code
A-Register = Actual Pattern
B-Register = Expected Pattern
Y-Register = Failure Address

4-20. REGISTER COMPLETION TEST (TST22)

Test 22 verifies proper operation of the hardware and firmware required to increment the A, B and X registers during the execution of the MEM map loading instructions.

This test includes six subtests, each of which executes one map loading instruction, and then verifies the correct value of the A, B, and X-registers. The six instructions used for this test are: XMM, XMS, SYA, USA, PAA, and PBA.

If an error is detected during the execution of this test, an error message will be output on the console and the program will halt the computer. At this time the operator will be able to determine the cause of the error by checking the following registers:

T-Register = Error Code
Y-Register = Error Address
* A-Register = Count at Completion
* B-Register = Count at Completion
* X-Register = Count at Completion

* If the error is A or B-register related, the failing register will contain the actual value, and the alternate register will contain the expected value. If the failure pertains to the X-register, the A-register will contain the expected value.

4-21. EXTENDED MEMORY TEST (TST23)

Test 23 is a utility program offered as a quick check of the lines required to have extended memory. It is not intended to be used as a thorough memory diagnostic, merely a verification of the hardware and firmware required to access memory sizes greater than 32K words.

This test starts by calculating memory size, builds a table of starting page numbers, and then executing one pass of address, complementary address, walking one and walking zero tests on all of extended memory. When all of the extended memory capability has been checked, control passes back to the main program.

If an error is detected during the execution of this test, no error message will be output on the console; however, a coded halt will occur so that the operator will be aware of the error and can determine the cause and address of the error by examining the following registers:

T-Register = Error Code
A-Register = Expected Data
B-Register = Actual Data
* X-Register = Logical Address of the Error

* To convert the logical memory address to a physical memory address, the operator must remember the following steps:

1. The logical page number is contained in memory address bits 10-14. Convert to an octal logical page number.

2. Select the corresponding map register. This can be done by selecting the M-register, setting bits 14 and 15 to one, and bits 0-9 to the address of the desired map register. Without pressing the STORE switch, select the T-Register. At this time, the T-register will contain the contents of the map register which was addressed by the M-Register. The contents of this map register is the physical memory page number.

4-22. BASIC I/O TEST (TST24)

Test 24 is a utility test which allows the operator to test the control and flag circuitry of the microcircuit interface PCA used for interrupts and DCPC transfers.

This test is not part of the standard tests (00-22), and should only be run to verify that the board is capable of DCPC transfers and/or interrupt when operator is having trouble in this are of the diagnostic, and suspects the trouble may be in the microcircuit interface PCA.

4-23. REGISTER CRUSHER TEST (TST25)

Test 25 is a utility test which allows the operator to extensively test the Random Access Memory used for the Map Registers.

Due to the rather lengthy execution time required to test for interaction between bits of every Map Register Address and bits of every other Map Register Address for every combination of bits, this test is not part of the standard tests (00-22) and should only be run if the operator suspects intermittent or "bit pattern sensitivity" problems with the Map Registers.

Test 25 begins with register 0 as the register under test, and for every combination of bits possible, tests for interference by writing all other registers with all combinations possible, checking each time to insure writing into other registers does not alter the contents of the register under test.

When register 0 has been tested in this manner with all other registers, Register 1 becomes the register under test and the above procedure is repeated for all combinations of bits and all other registers, then register 2 becomes the Register Under Test etc., until all 128 Registers have been tested then control is passed back to the executive.

Should an error occur during execution of TST25 an error message is output on the console, and the program halts the computer. At this time, the operator may determine the cause of the error halt, by checking the contents of the following registers:

T = Error Code
A = Actual Pattern
B = Expected Pattern
X = Failing Register
Y = Address of Failure

4-23. ERROR INFORMATION MESSAGE/HALT CODES

A halt code summary is given in table 4-1. Complete explanations of individual error information messages and halt codes appear in table 4-2.

Table 4-1. Error Code Summary

ERROR CODE	MEANING
Test 00-24	
102000-102067	Error(E) and Information(H) messages 00-67.
106000-106067	Error(E) and Information(H) messages 100-167.
103000-103067	Error(E) messages 200-267.
107000-107026	Error(E) and Information(H) messages 300-326.
Control	
102073	Select code input error.
102074	Select code input complete.
102075	User selection request.
102076	End of test (A = octal test number).
102077	End of diagnostic run.
106077	Trap cell halts in locations 2-77.
Note: See table 4-2 for complete explanation of individual halts.	

Table 4-2. Error Information Messages and Halt Codes

OCTAL CODE	MESSAGE	TEST	COMMENTS
None	MEMORY EXPANSION MODULE DIAGNOSTIC DSN = XXXXXX	ALL	Header message of diagnostic XXXXXX=Current DSN
None	PASS XXXXXX	ALL	End of pass message XXXXXX=Number in Octal.
102000	E000 CLF 0-SFC 0 ERROR	24	CLF/SFC 0 combination failed. CLF did not clear flag, or SFC caused no skip with flag clear.
102001	E001 CLF 0-SFS 0 ERROR	24	CLF/SFS 0 combination failed. CLF did not clear flag, or SFS caused skip with flag clear.
102002	E002 STF 0-SFC 0 ERROR	24	STF/SFC 0 combination failed. STF did not set flag, or SFC caused skip with flag set.
102003	E003 STF 0-SFS 0 ERROR	24	STF/SFS combination failed. STF did not set flag, or SFS caused no skip with flag set.
102004	E004 CLF 0 DID NOT INHIBIT INT	24	With card flag and control set, CLF 0 did not turn off interrupt system.
102005	E005 CLF CH-SFC CH ERROR	24	CLF/SFC CH combination failed. CLF did not clear flag or SFC caused no skip with flag clear.
102006	E006 CLF CH-SFS CH ERROR	24	CLF/SFS CH combination failed. CLF did not clear flag, or SFS caused skip with flag clear.
102007	E007 STF CH-SFC CH ERROR	24	STF/SFC combination failed. STF did not set flag, or SFC caused skip with flag set.
102010	E010 STF CH-SFS CH ERROR	24	STF/SFS combination failed. STF did not set flag or SFS caused no skip with flag set.

Table 4-2. Error Information Messages and Halt Codes (Continued)

OCTAL CODE	MESSAGE	TEST	COMMENTS
102011	E011 STF XX SET CARD FLAG	24	Select code screen test failed. A-register contains XX, where XX=select code that caused card flag to set.
102012	E012 INT DURING HOLD OFF INSTR	24	Interrupt occurred during an I/O instruction or a JMP/JSB,I instruction.
102013	E013 SECOND INT OCCURRED	24	Card interrupted a second time after initial interrupt was processed and interrupt system was turned back on.
102014	E014 NO INT	24	No interrupt occurred with card flag and control set and interrupt system on.
102015	E015 INT RTN ADDR ERROR	24	Interrupt did not store correct return address in memory.
102016	E016 CLC CH ERROR	24	CLC CH did not clear card control.
102017	E017 CLC 0 ERROR	24	CLC 0 did not clear card control.
102020	E020 PRESET DID NOT SET FLAG	24	PRESET did not set card flag.
102021	E021 PRESET DID NOT DISABLE INTS	24	PRESET did not disable interrupt system.
102022	E022 PRESET DID NOT CLEAR CONTROL	24	PRESET did not clear control.
102023	E023 PRESET DID NOT CLEAR I-O LINES	24	PRESET did not clear I/O data lines.
102024	H024 PRESS PRESET RUN	24	Press PRESET and RUN.
None	H025 BI-O COMP	24	

Table 4-2. Error Information Messages and Halt Codes (Continued)

OCTAL CODE	MESSAGE	TEST	COMMENTS
102026	E026 INT EXECUTION ERROR	24	Interrupt was not processed correctly and one or several instructions were processed incorrectly during the interrupt.
102030*	E030 XMS	01	Test 01's only error message.
102031*	E031 XMA	02	Check T, A, B, X, and Y-registers.
102032*	E032 XMB	02	Check T, A, B, X, and Y-registers.
102033*	E033 XMM	00	All map loading routines halt with the A, B, T, X, and Y-registers containing the following information: T=Error Code A=Pattern B=Pattern X=Register Number Y=Error Address Note: If the instruction that failed was a register reference instruction, the register referenced will contain the actual pattern, and the alternate register will contain the expected pattern.
102034*	E034 XMM	00	
102035*	E035 XMM	00	
102036*	E036 XMM	00	
102037*	E037 SYA	03	
102040*	E040 SYB	03	
102041*	E041 USA	03	
102042*	E042 USB	03	
102043*	E043 PAA	03	
102044*	E044 PAB	03	
102045*	E045 PBA	03	
102046*	E046 PBB	03	
102047*	E047 INTERFERENCE ERROR	25	Loading of one map interfered with contents of another.
102051	E050 DJP	04	DJP did not cause a JMP.

*For Register significance, see Test Descriptions.

Table 4-2. Error Information Messages and Halt Codes (Continued)

OCTAL CODE	MESSAGE	TEST	COMMENTS
102051	E051 DJS	04	DJS did not cause a JSB.
102052	E052 SJP	04	SJP did not enable or JMP.
102053	E053 SJS	04	SJS did not enable or JSB.
102054	E054 UJP	04	UJP did not enable or JMP.
102055	E055 UJS	04	UJS did not enable or JSB.
102056*	E056 JRS	04	JRS did not JMP.
102057	E057 JRS	04	JRS restored wrong status.
102060*	E060 SSM	04	SSM stored wrong status.
102061	E061 DJS	04	DJS stored incorrect return address for JSB.
102062	E062 SJS	04	SJS stored incorrect return address for JSB.
102063	E063 UJS	04	UJS stored incorrect return address for JSB.
102064*	E064 RSA	04	Unexpected RSA results for expected pattern.
102065*	E065 RSB	04	Incorrect RSB results.
102066*	E066 LFA	04	MEM fence register not changed by LFA or no interface board installed in specified sc.
102067*	E067 LFB	04	MEM fence register not changed by LFB.
103000	E200 DJP	13	DJP was not allowed with the System enabled.
103001	E201 DJS	13	PM allowed execution of DJS with User enabled.

*For Register significance, see Test Descriptions.

Table 4-2. Error Information Messages and Halt Codes (Continued)

OCTAL CODE	MESSAGE	TEST	COMMENTS
103002	E202 DJS	13	Privileged instruction bit was not set by DJS.
103003	E203 DJS	13	DJS was not allowed with System enabled.
103004	E204 SJP	13	PM allowed execution of SJP with User enabled.
103005	E205 SJP	13	Privileged instruction bit was not set by SJP.
103006	E206 SJP	13	SJP was not allowed with System enabled.
103007	E207 SJS	13	PM allowed execution of SJS with User enabled.
103010	E210 SJS	13	Privileged instruction bit was not set by SJS.
103011	E211 SJS	13	SJS was not allowed with System enabled.
103012	E212 UJP	13	PM allowed execution of UJP with User enabled.
103013	E213 UJP	13	Privileged instruction bit was not set by UJP.
103014	E214 UJP	13	UJP was not allowed with System enabled.
103015	E215 UJP	13	UJP not allowed with System enabled in PM.
103016	E216 UJS	13	PM allowed execution of UJS with User enabled.
103017	E217 UJS	13	Privileged instruction bit was not set by UJS.
103020	E220 UJS	13	Could not enable User in PM.
103021	E221 UJS	13	UJS not allowed with System enabled in PM.

Table 4-2. Error Information Messages and Halt Codes (Continued)

OCTAL CODE	MESSAGE	TEST	COMMENTS
103022	E222 XMA	14	XMA was allowed in PM.
103023	E223 XMA	14	Privileged instruction bit was not set by XMA.
103024	E224 LFA	13	LFA was allowed in PM.
103025	E225 LFA	13	Privileged instruction bit was not set by LFA.
103026	E226 XMM	14	XMM was allowed in PM.
103027	E227 XMM	14	Privileged instruction bit was not set by XMM.
103030	E230 XMS	14	XMS was allowed in PM.
103031	E231 XMS	14	Privileged instruction bit was not set by XMS.
103032	E232 SYA	14	SYA was allowed in PM.
103033	E233 SYA	14	Privileged instruction bit was not set by SYA.
103034	E234 USA	14	USA was allowed in PM.
103035	E235 USA	14	Privileged instruction bit was not set by USA.
103036	E236 PAA	14	PAA was allowed in PM.
103037	E237 PAA	14	Privileged instruction bit was not set by PAA.
103040	E240 PBA	14	PBA was allowed in PM.
103041	E241 PBA	14	Privileged instruction bit was not set by PBA.
103042	E242 NO DCPC FLAG AFTER 10 MS	15	DCPC did not respond to STC DCPC or no test connector on interface board.
103043*	E243 PORT A NOT ENABLED BY DCPC6	15	DCPC transfer was not a mapped transfer.

*For Register significance, see Test Descriptions.

Table 4-2. Error Information Messages and Halt Codes (Continued)

OCTAL CODE	MESSAGE	TEST	COMMENTS
103044	E244 PORT B NOT ENABLED BY DCPC7	15	DCPC transfer was not a mapped transfer.
103045	E245 MWW	16	MWW did not cause a Read Violation.
103046	E246 MWW	16	MWW did not set Read Violation bit.
103047	E247 MWI	16	MWI did not cause a Read Violation.
103050	E250 MWI	16	MWI did not set Read Violation bit.
103051	E251 MBW	16	MBW did not cause a Read Violation.
103052	E252 MBW	16	MBW did not set Read Violation bit.
103053	E253 MBI	16	MBI did not cause a Read Violation.
103054	E254 MBI	16	MBI did not set Read Violation bit.
103055	E255 MBF	17	MBF did not execute correctly when interrupted.
103056	E256 MBW	17	MBW did not execute correctly when interrupted.
103057	E257 MWF	17	MWF did not execute correctly when interrupted.
103060	E260 MWI	17	MWI did not execute correctly when interrupted.
103061	E261 MWW	17	MWW did not execute correctly when interrupted.
103062	E262 XMS	17	XMS did not execute correctly when interrupted.

*For Register significance, see Test Descriptions.

Table 4-2. Error Information Messages and Halt Codes (Continued)

OCTAL CODE	MESSAGE	TEST	COMMENTS
103063	E263 XMM	17	XMM did not execute correctly when interrupted.
103064*	E264 DCPC	20	DCPC interference.
103065	E264 MBI	17	MBI did not execute correctly when interrupted.
103066	E266 NO INTP, ABORTING TEST	17	No interrupt was detected which is mandatory.
103067	E267 DCPC	20	DCPC did not initiate a transfer.
106000*	E100 XSA	05	No X-store, or incorrect results of X-store.
106001*A	E101 XLA	05	Incorrect results of X-load. A=actual, B=expected, and Y=address of failing instruction
106002*A	E102 XCA	05	Incorrect X-compare results or no P+1 if compare was made.
106003*	E103 XSA	05	XSA into System failed.
106004*A	E104 XLA	05	XLA from System failed.
106005*A	E105 XCA	05	XCA into System failed.
106006*	E106 XSB	05	XSB into User failed.
106007*A	E107 XLB	05	XLB from User failed.
106010*A	E110 XCB	05	XCB with User failed.
106011	E111 XSB	05	XSB into System failed.
106012*A	E112 XLB	05	XLB into User failed.
106013*A	E113 XCB	05	XCB with System failed.

These error halts will be reached if ROM Part No. 13307-80033 through 13307-80035 are installed in the HP 1000 E/F-Series Computer. Cross compare errors (E102, E105, E110 & E113) will however not show a difference in the expected vs the actual data pattern. These instructions are only needed in RTE IV.

Table 4-2. Error Information Messages and Halt Codes (Continued)

OCTAL CODE	MESSAGE	TEST	COMMENTS
106014	E114 PM NOT SET BY STC 05	10	Protected mode status not detected after STC 05.
None	H115 PRESS HALT-PRESET-RUN IN LESS THAN 10 SECONDS	10	
106016	E116 PM OR MEM FENCE NOT CLEARED BY PRESET	10	The MEM fence or PM status was not cleared by preset.
None	H117 PRESET TEST COMPLETE	10	
106020	E120 RDV — MPT VIOLATION	ALL	A Memory Protect violation was detected when an MEM read violation was forced.
106021	E121 WTV — MPT VIOLATION	ALL	A Memory Protect violation was detected when a MEM write violation was forced.
106022*	E122 MWF	GG	Move from User failure.
106023*	E123 MWF	06	Move from System failure.
106024*	E124 MWI	06	Move into User failure.
106025*	E125 MWI	06	Move into System failure.
106026*	E126 MWW	06	Move within User failure.
106027*	E127 MWW	06	Move within System failure.
106030*	E130 MBF	07	Move from User failure.
106031*	E131 MBF	07	Move from System failure.
106032*	E132 MBI	07	Move into User failure.
106033*	E133 MBI	07	Move into System failure.
106034*	E134 MBW	07	Move within User failure.
106035*	E135 MBW	07	Move within System failure.

*For Register significance, see Test Descriptions.

Table 4-2. Error Information Messages and Halt Codes (Continued)

OCTAL CODE	MESSAGE	TEST	COMMENTS
106036	E136 NO READ MEMV	11	No Read Violation reported by MEM when Read Violation was forced.
106037	E137 NO WRITE MEMV	11	No Write Violation reported by MEM when a Write Violation was forced.
106040	E140 PM ALLOWED WRITE	11 10	Protected Mode did not stop memory contents from being altered.
106041	E141 NO BP MEMV	11	No Violation reported trying to access under MEM Base Page Fence.
106042	E142 JMP ALLOWED WITHIN BPF	11	Base Page Fence allowed program to jump within its boundaries.
106043	E143 PM ALLOWED READ	11	A load from protected memory was allowed after violation.
106044	E144 RVA	11	Unexpected RVA results. The B-register=expected violation register content and the Y-register=the address of the failure.
106045*	E145 RVB	11	Unexpected RVB results. The A-register has the expected value, and the Y-register has the address of the failure.
106046*	E146 RVA	11	Same as hlt 106044.
106047*	E147 RVA	11	Same as HLT 106044.
106050*	E150 RVA	11	Same as HLT 106044.
106051	E151 MBI	12	MBI did not cause a MEMV in Protected mode.

*For Register significance, see Test Descriptions.

Table 4-2. Error Information Messages and Halt Codes (Continued)

OCTAL CODE	MESSAGE	TEST	COMMENTS
106052*	E152 MBI	12	MBI did not set the Write Violation bit after an illegal write operation.
106053	E153 MBW	12	MBW did not cause an MEMV in Protected Mode.
106054*	E154 MBW	12	MBW did not set Write Violation bit.
106055	E155 MWI	12	MWI did not cause an MEMV in Protected Mode.
106056*	E156 MWI	12	MWI did not set Write Violation bit.
106057	E157 MWW	12	MWW did not cause an MEMV in Protected Mode.
106060*	E160 MWW	12	MWW did not set Write Violation bit.
106061*	E161 XSA	12	XSA did not cause an MEMV in Protected Mode.
106062*	E162 XSA	12	Write Violation bit was not set by XSA.
106063	E163 JRS	13	PM allowed execution of JRS with User enabled.
106064*	E164 JRS	13	Privileged instruction bit was not set by JRS.
106065	E165 JRS	13	JRS was not allowed with System enabled.
106066	E166 DJP	13	PM allowed execution of DJP with User enabled.
106067*	E167 DJP	13	Privileged instruction bit was not set by DJP.

*For Register significance, see Test Descriptions.

Table 4-2. Error Information Messages and Halt Codes (Continued)

OCTAL CODE	MESSAGE	TEST	COMMENTS
107000	E300 PIV — MPT VIOLATION	ALL	A Memory Protect Violation was detected when a MEM Privileged Instruction Violation was forced.
107001*	E301 VR MAP 15	21	Violation register map bits incorrect.
107002*	E302 VR MAP 00	21	Violation register map bits incorrect.
107113*	E303 VR MAP 11	21	Violation register map incorrect page 0
107004*	E304 A-REG	22	A-register incorrect after XMM.
107005*	E305 B-REG	22	B-register incorrect after XMM.
107006*	E306 X-REG	22	X-register incorrect after XMM.
107007*	E307 A-REG	22	A-register incorrect after XMS.
107010*	E310 B-REG	22	B-register incorrect after XMS.
107011*	E311 X-REG	22	X-register incorrect after XMS.
107012*	E312 A-REG	22	A-register incorrect after SYA.
107013*	E313 A-REG	22	A-register incorrect after USA.
107014*	E314 A-REG	22	A-register incorrect after PAA.
107015*	E315 A-REG	22	A-register incorrect after PBA.
107016*	E316 VR MAP 12	21	Violation map incorrect.
None	H317 MUST HAVE GREATER THAN 32K	23	Extended memory test was selected with less than 32K of available memory. Control exits back to the main program.

*For Register significance, see Test Descriptions.

Table 4-2. Error Information Messages and Halt Codes (Continued)

OCTAL CODE	MESSAGE	TEST	COMMENTS
107020	No message	23	A failure was detected while running address or complementary address test. At this time, the A-register will contain expected data pattern, B-register will contain actual data pattern, and X-register will contain address of failure. When Extend register is clear, the address test is being run, and when Extend register is set, the address complement is being run.
107021*	No message	23	Walking one test failure. A=expected pattern, B=actual pattern, and X=address of failure.
107022*	No message	23	Information halt used to display address of error which caused above halt (107021).
107023	E232 NO BP MEMV	11	Trying to store within Base Page protected area did not cause MEMV.
107024*	E324 RVA	11	Violation Register bit 13 not set by base page violation.
107025	E325 M-E BUS	23	Memory expansion bus failure.
107026	No message	10	Used to inform operator with no console that the Preset Test is next.
107027	H327 XXK OF CONTIGUOUS MEMORY INSTALLED	23	Displays the memory size installed (32K or above) of contiguous memory.

*For Register, significance, see Test Descriptions.

APPENDIX A

The information contained in this appendix is intended for use as HP 2000 Hardware Support Data in the Customer Support Handbook, HP part no. 5951-7357. The text is outlined so that it can be cut out around the outline and, after holes are punched at the indicated crosses, the pages can be inserted in the six ring binder under the appropriate manual section.

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HP 12976A DYNAMIC MAPPING SYSTEM
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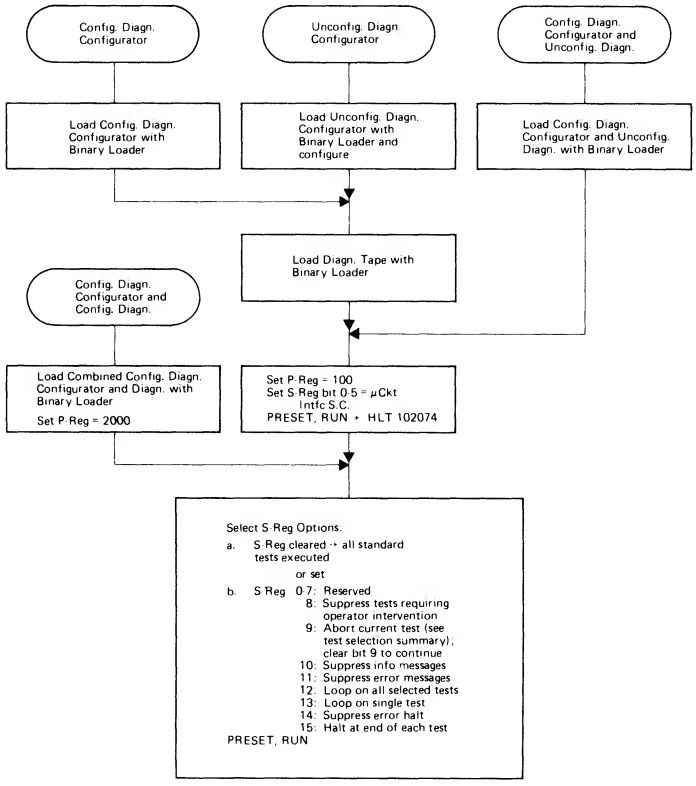

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